REMARKS/ARGUMENTS

Claims 2-9 and 12-20 are currently pending in the present patent application, with claims 1 and 11 having been cancelled in previous amendments. Claim 3, 8-9, 12 and 14 are currently amended. Claim 10 is hereby canceled without prejudice or disclaimer.

Consideration of Cited Reference

Applicants' attorney notes that the Examiner has yet to indicate consideration of the reference EP 0 295 751 A1, filed in English via information disclosure statement on November 12, 2003. Applicants' attorney respectfully requests that the Examiner indicate consideration of this reference at the Examiner's earliest convenience.

Objections to the Specification

In Section 3 of the Office Action mailed on April 2, 2009, in the above-referenced patent application, the Examiner maintains his objections to the specification because the title of the invention appears to be misleading. Applicants thank the Examiner for his comments and have amended the title as recommended.

Objections to the Claims

In Section 7 of the Office Action, the Examiner objects to claim 8. Claim 8 recites "a control circuit coupled to the memory locations". However, it appears that the claim should read "a control circuit coupled to the memory". Claim 8 has been amended to correct this non-substantive error.

Rejections Under 35 U.S.C. § 112

In Section 9 of the Office Action, the Examiner maintains his rejections of claim 10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claim 10 is hereby canceled without prejudice or disclaimer.

Rejections Under 35 U.S.C. § 102

In Section 10 of the Office Action, the Examiner rejects claims 8-9 and 14-16 under 35 U.S.C. § 102(e) as being anticipated by US Patent No. 6,578,109 to Stone et al. ("Stone").

Claim 8 as amended recites a memory including a plurality of memory locations and a control circuit coupled to the memory and operable to provide random access to the memory locations responsive to a read operation, and to provide sequential access to the memory locations responsive to a write operation.

In contrast, Stone does not disclose a control circuit operable to provide random access to memory locations responsive to a read operation and to provide sequential access to the memory locations responsive to a write operation. Referring, *e.g.*, to FIG. 10 and column 9 line 43 through column 10 line 12, Stone allows both read operations and write operations to occur using either random access or sequential access. This approach may require additional overhead circuit in the memory device as well as additional operational cycles of the memory control circuit, which embodiments of the present invention can avoid.

Stone does not satisfy the combination of limitations recited in claim 8, and Applicants' attorney respectfully requests that the rejection be withdrawn accordingly. Claim 14 as amended is patentable at least for the reasons described above with respect to claim 8. Claims 9 and 15-16 are patentable at least by virtue of their respective dependencies from one of independent claims 8 and 14 and due to the additional limitations added by each of these dependent claims.

Rejections Under 35 U.S.C. § 103

Claim 10

In Section 13 of the Office Action, the Examiner rejects claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Stone and well known practice in the art. As noted above, claimed 10 has been canceled without prejudice or disclaimer.

Claims 8 and 14-16

In Section 14 of the Office Action, the Examiner rejects claims 8 and 14-16 under Section 103(a) as being unpatentable over US Patent Publication No. 2002/0087817 to Tomaiuolo ("Tomaiuolo") and US Patent No. 4,656,625 to Nojiri ("Nojiri").

Claim 8 recites a memory including a plurality of memory locations and a control circuit coupled to the memory locations and operable to provide random access to the memory locations during a read mode of operation and provide sequential access to the memory locations during a write mode of operation.

As the Examiner acknowledges on page 7 of the instant Office Action, Tomaiuolo does not disclose a memory that provides random access to memory locations during read operations while providing sequential access to memory locations during write operations. Sequential or random access in Tomaiuolo is determined not based upon whether the operation is a read or write operation, but rather upon the addresses of the memory locations being accessed. Thus, Tomaiuolo does not disclose or reasonably suggest providing random access to memory locations during read accesses and sequential access during write accesses.

Nojiri discloses a telecommunications switching system that includes a mixing circuit, a feedback circuit, and a speech path memory operative to store voice data signals provided from subscribers holding a conference. With respect to the speech path memory, Nojiri discloses that "read and write operations . . . are achieved under a random read and sequential write mode," but does not describe how these operations are achieved.

In fact, because the description of the speech path memory is so abstract in comparison to the circuit-level memory device described by Tomaiuolo, it is unclear how one would go about combining them. Nojiri and Tomaiuolo are completely non-analogous art. Tomaiuolo discloses a circuit-level memory device; Nojiri teaches a telecommunications switching system that, although it employs memory devices, does not describe memory operations or structure at a level that one would be able to combine with the memory device taught by Tomaiuolo.

The Examiner asserts that combining the teachings of Nojiri and Tomaiuolo would be obvious "because doing so would have permitted simultaneous communication between multiple requesters." This motivation is nonsensical with respect to both the present application and Tomaiuolo, neither of which is concerned with either simultaneous communication or multiple requesters.

Neither Tomaiuolo nor Nojiri, either alone or in combination, disclose or render obvious the limitations of claim 8. Independent claims 14-15 are patentable for at least the same reasons described above with respect to claim 8. Claim 16 is patentable at least by virtue of its dependency from independent claim 15 and due to the additional limitations added by this dependent claim.

Claims 2-7

In Section 15 of the Office Action, the Examiner rejects claims 2-7 under § 103(a) as being unpatentable over US Patent No. 6,091,645 to Iadanza ("Iadanza"), Applicant Admitted Prior Art ("APA"), and Stone.

Independent claim 3 as amended recites, in relevant part, a memory including at least one array of memory elements and a partition of the at least one array into a plurality of sub-arrays of the memory elements and an array configuration circuit for selectively placing the at least one array into one of two operating configurations. The first operating configuration is a data storage configuration into which the memory is placed when data are to be stored therein, and the second operating configuration is a

data retrieval configuration into which the memory is placed when data are to be retrieved therefrom.

Iadanza discloses a memory that can be configured to operate in various modes, such as RAM, FIFO, and LIFO (see col. 2, lines 28-36). Iadanza teaches, however, that each sub-array 12 (Figure 1A) is "programmed into, and thereafter accessed using, one of a set of modes." Id. As the Examiner implicitly acknowledges on page 9 of the instant Office Action, Iadanza neither discloses nor suggests a memory array or sub-array operating in different modes based upon whether the access of the memory is a read or write operation. Each sub-array is configured to operate in a set mode, and this mode does not vary depending upon whether the sub array is being accessed for a read or a write operation.

Also on page 9 of the instant Office Action, the Examiner cites paragraphs 6-7 of the instant application to show that the APA discloses a first operating configuration in which memory elements of an array are coupled to one another to form a mono dimensional sequentially-accessible memory, and a second operating configuration in which memory elements within each sub-array are coupled to one another so as to form an independent sequentially-accessible memory block. In this way, the Examiner asserts, the APA discloses a memory that can be accessed sequentially in a FIFO manner or accessed randomly. Respectfully, this is incorrect. Referring, *e.g.*, to paragraphs 6-7, the APA discusses FIFO memories and randomly-accessible memories, but does not disclose a memory that is configurable between those two options as separate modes of operation. In fact, specifically referring to paragraph 4 of the APA, the APA clearly indicates that designers are normally forced to *choose* between implementing a memory block or blocks as FIFO memories or as randomly accessible.

As the Examiner appears to acknowledge on page 10 of the instant Office Action, neither Iadanza nor the APA discloses that the first operating configuration is a data storage configuration, in which the memory is forced when data are to be stored

therein, and the second operating configuration is a data retrieval configuration, in which the memory is forced when data are to be retrieved therefrom.

Stone does not provide the missing teaching. As analogously discussed above with respect to the rejections applying Stone under § 102(e), Stone neither discloses nor suggests placing a memory into one of two operating configurations depending on whether data is being stored therein or retrieved therefrom. Stone allows both read operations and write operations to occur using either random access or sequential access. This approach may require additional overhead circuitry, as well as additional cycles of the memory control circuit, that embodiments of the present invention can avoid.

In sum, neither Iadanza, the APA, or Stone, either alone or in combination, disclose or reasonably suggest the combination of limitations of claim 3. Claims 2 and 4-7 are patentable at least by virtue of their respective dependencies from claim 3 and due to the additional limitations added by these dependent claims.

Claims 12-13

In Section 16 of the Office Action, the Examiner rejects claims 12-13 under Section 103(a) as being unpatentable over Tomaiuolo, Iadanza and Stone.

Claim 12 as amended recites a memory including an array of memory locations; and a control circuit coupled to the array and operable to cause the array to operate as a random access memory during all read operations and a first in first out memory during all write operations. The memory locations comprise rings of serially coupled memory locations, each having a respective contents, with the contents of each ring being independent of the contents of the other rings. During the read mode of operation, the control circuit is operable to control each of the rings to receive a clock signal, shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and

allow access to one of the memory locations during a predetermined cycle of the clock signal.

As the Examiner acknowledges on page 14 of the instant Office Action, neither Tomaiuolo and Iadanza, alone or in combination, discloses operating as a random access memory during reads and a FIFO memory during writes.

As analogously discussed above, Stone neither discloses nor reasonably suggests a control circuit operable to cause a memory array to operate as a random-access memory during all read operations, and as a first-in-first-out memory during all write operations. The modes of access employed by Stone are not determined simply by whether a given operation is a read operation or a write operation.

For at least these reasons, the combination of elements recited in independent claim 12 is allowable. Dependent claim 13 is allowable for at least the same reasons as claim 12 and due to the additional limitations added by this dependent claim.

Claims 17-20

In Section 17 of the Office Action, the Examiner rejects claims 17-20 under Section 103(a) as being unpatentable over Stone and Iadanza.

These claims are patentable at least by virtue of their respective dependencies from independent claim 15, discussed above, and due to the additional limitations added by each of these dependent claims.

CONCLUSION

The absence of additional patentability arguments should not be construed as either a disclaimer of such arguments or that such arguments are not believed to be meritorious. The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **Should the Examiner have any further questions about the application, Applicants respectfully request the Examiner to contact the undersigned attorney at (425) 455-5575 to arrange for a telephone interview to discuss the outstanding issues.** If the need for any fee in addition to any fee paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,
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